Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-5 (cancelled)

Claim 6 (previously presented): A method of receiving a signal, comprising:

comparing an input voltage to a first reference voltage;

comparing said input voltage to a second reference voltage, wherein either said first reference voltage or said second reference voltage is active;

selecting an output voltage based on said the difference between said input voltage and the active reference voltage of either said first reference voltage or said second reference voltage;

changing said output voltage when said input voltage crosses said activated reference voltage; and

changing the activated reference voltage when said input crosses said activated voltage.

Claim 7 (previously presented): The method of claim 6, further comprising:

holding said output voltage for a period of time without regard to said input voltage crossing said activated reference voltage.

Claims 8 and 9 (cancelled)

Claim 10 (previously presented): An apparatus, comprising:

a first comparator that compares a first reference voltage to an input signal, said first comparator comprising a first comparator output;

a second comparator that compares a second reference voltage to said input signal, said second comparator comprising a second comparator output;

a selector comprising at least one selector input, a selector output, and a selector control, said at least one selector input being connected to said first comparator output and said second comparator output, said selector passing the voltage of one of said first comparator output and said second comparator output to an output of said apparatus via said selector output depending upon which of said first reference voltage and said second reference voltage is activated; and

an activator/deactivator comprising at least one input and at least one output, said at least one input being operatively connected to said first comparator output and said second comparator output, said at least one output being operatively connected to said selector control, said activator/deactivator controlling said selector depending upon the state of said first output and said second output.

Claim 11 (currently amended): The apparatus of claim 10, comprising

a holder that prevents said receiver output from changing for a period of time after a change in which either one of said first reference voltage ~~and~~ or said second reference voltage is activated and the other reference voltage is deactivated.

Claims 12-15 (cancelled)

Claim 16 (previously presented): The apparatus of claim 11, wherein said holder comprises a delay circuit.

Claim 17 (previously presented): The apparatus of claim 11, wherein said holder comprises a at least two inverters, wherein an input of a first inverter is connected to the output of a second inverter and the output of said first inverter is connected to the input of said second inverter.

Claim 18 (previously presented): The apparatus of claim 10, wherein said selector is a multiplexor.

Claim 19 (previously presented): The apparatus of claim 10, wherein said activator/deactivator is a flip-flop circuit.

Claim 20 (previously presented): An electronic circuit comprising:

a first comparator comprising a first comparator first input, a first comparator second input, and a first comparator output, said first comparator first input being connectable to an input voltage, said first comparator second input being connected to a first reference voltage;

a second comparator comprising a second comparator first input, a second comparator second input, and a second comparator output, said second comparator first input being connectable to an input voltage, said second comparator second input being connected to a second reference voltage, said second reference voltage being less that said first reference voltage;

an AND gate, wherein a first input of said AND gate is connected to said first comparator output and a second input of said AND gate is connected to said second comparator output;

a NOR gate, wherein a first input of said NOR gate is connected to said first comparator output and a second input of said NOR gate is connected to said second comparator output;

a flip-flop circuit comprising a flip-flop first input that is connected to the output of said AND gate, a flip-flop second input that is connected to the output of said NOR gate, and a flip-flop output; and

a multiplexor comprising a multiplexor first input that is connected to said first comparator output, a multiplexor second input that is connected to said second comparator output, a muliplexor control that is connected to said flip-flop output, and a multiplexor output that is the output of said electronic circuit.

Claim 21 (previously presented): The electronic circuit of claim 20 and further comprising:

a delay circuit, where an input of said delay circuit is connected to said flip-flop output;

an exclusive NOR gate, wherein a first input of said exclusive NOR gate is connected to said flip-flop output and wherein a second input of said exclusive NOR gate is connected to an output of said delay circuit; and

a switch comprising a switch input, a switch output, and a switch control, said switch input being connected to said multiplexor output, said switch output being the output of said electronic circuit, said switch control being connected to the output of said exclusive NOR gate.

Claim 22 (previously presented): The electronic circuit of claim 20 and further comprising a holding circuit operatively connected to said switch output.